IN THE CLAIMS

Please amend the claims to be in the form as follows:

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Claim 1 (currently amended): A data processing system which may be situated in a reduced-power mode, comprising a first data processing unit that has access to a memory belonging to the first data processing unit and a second data processing unit that has access to the memory belonging to the first data processing unit,
characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system.

Claim 2 (currently amended): A data processing system as claimed in Claim 1,
characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a period of time in which the reduced-power mode of the data processing system implies a reduced-power mode of the first data processing unit.

Claim 3 (previously amended): A data processing system as claimed in Claim 1,
characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit when a memory belonging to the second data processing unit is switched off.

Claim 4 (previously amended): A system as claimed in Claim 1,
characterized in that the memory belonging to the first data processing unit forms part of the first data processing unit.

Claim 5 (previously amended): A system as claimed in Claim 1,
characterized in that the memory belonging to the first data processing unit is a cache memory.

Claim 6 (previously amended): A system as claimed in Claim 1,
characterized in that the first data processing unit is a microprocessor.

Claim 7 (previously amended): A system as claimed in Claim 1, characterized in that the second data processing unit is a video controller.

Claim 8 (original): A data processing unit having access to a memory belonging to the data processing unit which data processing unit may be situated in a reduced-power mode, characterized in that the data processing unit is arranged for offering access in the reduced-power mode to the memory belonging to the data processing unit.

B1 Claim 9 (new): A data processing system as claimed in Claim 8, further comprising a mechanism that allows the first data processing unit to offer a second data processing unit access to the memory belonging to the first data processing unit in the reduced-power mode.

Claim 10 (new): A data processing system as claimed in Claim 9, wherein the second memory unit can be accessed by system components other than the first or second data processing units in the reduced-power mode.

Claim 11 (new): A data processing system as claimed in Claim 9, wherein the first data processing unit is arranged for offering the second data processing unit access to the first memory when the second memory is switched off.

Claim 12 (previously amended): A data processing system as claimed in Claim 9, wherein that the memory belonging to the first data processing unit is a cache memory.

Claim 13 (new): A data processing system which may be situated in a reduced-power mode having a first data processing unit that has access to a first memory associated with the first data processing unit and a second data processing unit that has access to the first memory comprising:

a second memory associated with the second data processing unit; and

a mechanism that allows the first data processing unit to offer the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system.

Claim 14 (new): A data processing system as claimed in Claim 13, wherein the second memory unit can be accessed by system components other than the first or second data processing units in the reduced-power mode.

Claim 15 (new): A data processing system as claimed in Claim 13, wherein the first data processing unit is arranged for offering the second data processing unit access to the first memory when the second memory is switched off.

Claim 16 (new): A system as claimed in Claim 13, wherein the memory belonging to the first data processing unit forms part of the first data processing unit.

Claim 17 (new): A system as claimed in Claim 13, wherein the memory belonging to the first data processing unit is a cache memory.

Claim 18 (new): A system as claimed in Claim 13, wherein the first data processing unit is a microprocessor.

Claim 19 (new): A system as claimed in Claim 13, wherein the second data processing unit is a video controller.